



Document No.: 4066 D1/Consilium/DV

PATENT/OFFICIAL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

John F. ARACKAPARAMBIL et al.

Serial No. 10/084,092

Filed: February 28, 2002

: Group Art Unit: 2121

: Examiner:

For: COMPUTER INTEGRATED MANUFACTURING TECHNIQUES

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

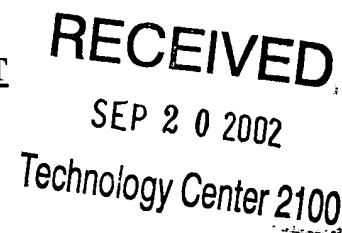
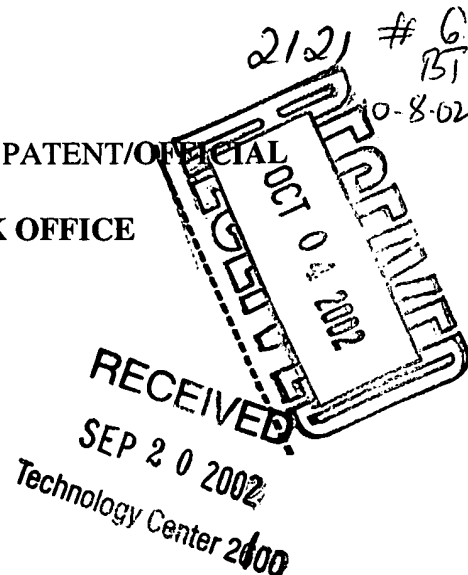
Honorable Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom. Copies of the references listed on pages 1 and 2 of Form PTO-1449 are submitted herewith.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

This submission does not constitute a representation that a search has been made or that no better art exists and does not constitute an admission or representation that any of the listed documents is material or constitutes prior art. If it should be determined that any of the listed documents does not constitute prior art under the United States law, Applicants reserve the right



Serial No. 10/084,092

to present to the Office the relevant facts and law regarding the appropriate status of such document.

No certification or fee is believed to be required. However, the Commissioner is hereby authorized to charge any additional fees should any be required for this submission, or credit any overpayment to deposit account no. 08-0219.

Respectfully submitted,

HALE AND DORR LLP



Scott M. Alter

Registration No. 32,879

1455 Pennsylvania Avenue, NW
Washington, DC 20004
TEL 202.942.8428 SMA:lrr
FAX 202.942.8484
Date: 9/19/02

**INFORMATION DISCLOSURE
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(PTO-1449)

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Technology Center 2100

APPLICANT
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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,698,766	10/06/87	Entwistle et al.			05/17/85
	4,967,381	10/30/90	Lane et al.			07/06/89
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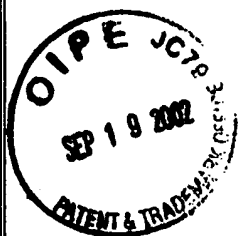
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
	61-171147	08/01/86	Japan				X
	6-184434	07/05/94	Japan				X
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	February 1984. "Method and Apparatus of in Situ Measurement and Overlay Error Analysis for Correcting Step and Repeat Lithographic Cameras." <i>IBM Technical Disclosure Bulletin</i> , pp. 4855-4859.
	October 1984. "Method to Characterize the Stability of a Step and Repeat Lithographic System." <i>IBM Technical Disclosure Bulletin</i> , pp. 2857-2860.
EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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	Schmid, Hans Albrecht. 1995. "Creating the Architecture of a Manufacturing Framework by Design Patterns." Austin, Texas: OOPSLA.
	Baliga, John. July 1999. "Advanced Process Control: Soon to be a Must." Cahners Semiconductor International. www.semiconductor.net/semiconductor/issues/issues/1999/jul99/docs/feature1.asp

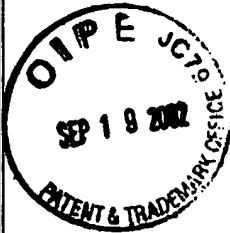
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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)				ATTY. DOCKET NO. 4066 D1/Consilium/DV		SERIAL NO. 10/084,092	
				RECEIVED SEP 20 2002 Technology Center 2100			
				APPLICANT John F. ARACKAPATHAMBI, et al.		FILING DATE February 28, 2002	
				GROUP 2121			
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						Yes	No
	11-135601	05/21/99	Japan				X
	WO 00/05759	02/03/00	WO			X	
	WO 00/35063	06/15/00	WO			X	
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	6,303,395	10/16/01	Nulman			06/01/99	
	6,345,315	02/05/02	Mishra			08/12/98	
	6,366,934	04/02/02	Cheng et al.			06/02/99	
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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
	WO 00/79355 A1	12/28/00	WO			X	
	2001-76982	03/23/01	Japan				X
	WO 01/33501 A1	05/10/01	WO			X	
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